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APPLICATION NO	).	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/803,693		03/18/2004	, S. Brandon Keller	200311777-1	7814	
22879	7590	03/27/2006		EXAMINER		
		KARD COMPAN	KIK, PHALLAKA			
P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION				ART UNIT	PAPER NUMBER	
FORT CO	LLINS, (	CO 80527-2400		2825		
				DATE MAILED: 03/27/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)				
		10/803,693	KELLER ET AL.				
	Office Action Summary	Examiner	Art Unit				
		Phallaka Kik	2825				
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence address				
WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DATE of the may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. The preriod for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONEI	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status							
1)⊠	Responsive to communication(s) filed on 18 M	arch 2004.					
2a)□	This action is <b>FINAL</b> . 2b)⊠ This	action is non-final.					
3)[	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
	closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	33 O.G. 213.				
Dispositi	ion of Claims						
5)□ 6)⊠ 7)□	Claim(s) <u>1-33</u> is/are pending in the application. 4a) Of the above claim(s) is/are withdraw Claim(s) is/are allowed. Claim(s) <u>1-33</u> is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or	vn from consideration.					
Applicati	ion Papers						
10)⊠	The specification is objected to by the Examine The drawing(s) filed on <u>18 March 2004</u> is/are: Applicant may not request that any objection to the Replacement drawing sheet(s) including the correction of the oath or declaration is objected to by the Examine	a)⊠ accepted or b)⊡ objected to drawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). sected to. See 37 CFR 1.121(d).				
Priority u	ınder 35 U.S.C. § 119						
a)[	Acknowledgment is made of a claim for foreign All b) Some * c) None of:  1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureausee the attached detailed Office action for a list of the certified copies of the priorical bureause the attached detailed Office action for a list of the certified copies of the priorical bureause the attached detailed Office action for a list of the certified copies of the priorical bureause the attached detailed Office action for a list of the certified copies of the priorical bureause the attached detailed Office action for a list of the certified copies of the priorical bureause the certified copies of the certified copies of the priorical bureause the certified copies of the priorical bureause the certified copies of the certified	s have been received. s have been received in Application tity documents have been received (PCT Rule 17.2(a)).	on No ed in this National Stage				
Attachmen		a.□	(770.440)				
2) D Notic 3) Inforr	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date 3/18/04.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

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### **DETAILED ACTION**

This Office Action responds to the Application and IDS filed on 3/18/2004.
 Claims 1-33 are pending.

## Specification

2. The disclosure is objected to because of the following informalities:

the referenced U.S. application numbers are missing (see page 1 of Applicant's specification).

Appropriate correction is required.

## Claim Objections

3. Claims 12-19,26-30 are objected to because of the following informalities:

As per **claim 12**, "second" (line 10) should be --external-- for proper antecedent basis.

As per **claims 13-19**, the claims are objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 26**, "second" (line 12) should be --external-- for proper antecedent basis.

As per claim 28, "are flattened" (line 4) should deleted for proper grammar.

As per **claims 27-30**, the claims are objected to for incorporating the above errors into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

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4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claims 1-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor et al. (U.S. Patent No. 5,815,402).

As per claims 1,7-9,12,20-21,25-26,31-33, all of the elements of the claims are illustrated in Figs. 7 and 9, wherein the flat netlist driver (710) reads or traverse the logical representation of the hierarchical design (i.e., schematic netlist) (see steps 904-920 of Fig. 9), which includes reading/loading determining the RC information as parameters (see col. 10, lines 31-42; col. 8, lines 13-47), wherein the flat netlist formatter writes the flat representation of each instantiation to the flat netlist file (col. 10, line 43 to col. 11, line 49), for use by other tools (i.e., other software and tools used by other designers--col. 1, lines 49-68; Fig. 8, showing at least simulator software. schematic design tool to which the flat netlist is accessible), wherein such flat netlist files can be considered as external since it is at least external to the flat netlist driver and is accessible by other tools or processes; wherein the computer readable medium operable with a computer, containing computer-executable instructions for implementing the method, the system, and the means associated with the system are part of the CAD system (see col. 6, lines 30-47; Fig. 6), being necessary to implement the computerimplemented method.

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As per **claims 2,13,27**, all of the elements of claims 1,12,26, from which the claims depend, are discussed in the rejections of claims 1,12,26 above, wherein the deleting of the information for the block from the RC model are also described in col. 22, line 62-67 and col. 24, lines 31-65.

As per claims 3-5,10,14-16,28-30, all of the elements of claims 1,7,12,26, from which the respective claims depend, are discussed in the rejections of claims 1,7,12,26 above, wherein the particular order of flattening the hierarchical design and the different levels of hierarchy being process are also illustrated in Fig. 9, showing a top-down flow, from top blocks to lower blocks (i.e., flattening first hierarchical level first before next hierarchical level) and performing all of the blocks of a particular net or group being selected before going to a different net or group.

As per claims 6,11,19,24, all of the elements of claims 1,7,12,20, from which the respective claims depend, are discussed in the rejections of claims 1,7,12,20 above, wherein the storage capacity of the second analysis tool/system is greater than the storage capacity of the first circuit analysis tool is within the scope of the prior art because the flattened file is inherently larger than the hierarchical file and any processing tool/system that processes the larger file (i.e., the flattened file) must necessarily have greater storage or memory capacity than that of the tool/system processing the smaller file (i.e., hierarchical file) in order for the that tool/system to process the required amount of data.

As per claims 17-18,22-23, all of the elements of claims 12,20, from which the respective claims depend, are discussed in the rejections of claims 12,20 above,

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wherein the storage devices for storing logical representation and RC model are also in Fig. 6 as part of the storage of the computer system for which the circuit design files (i.e., schematic file, netlist files) are stored.

### Conclusion

- 6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action.
- 7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 8:30AM-7PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik

U.S. Patent Examiner

March 18, 2006